Overcoming Planar MOSFET Scaling Barriers Using 3D FinFET Technology

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Abstract— Evolution of electronics has brought down the size of a transistor from millimeter to micrometer scale. Since Moore's law driven scaling of transistors, downscaling came to nanometer range. This huge downscaling is the result of invention of MOSFET and corresponding reduction in its channel length. The undesirable secondary effects masked the primary advantages of MOSFETs. There arose the requirement of thinking on new way for transistor structure. This results the path for the non – planar FinFETs. FinFETs have emerged as successors of MOSFETs. Owing to the presence of multiple gates, FinFETs are able to tackle short-channel effects (SCEs) better than conventional planar MOSFETs at deeply scaled technology and thus enable continued transistor scaling. This paper provides the background, characteristics and comparison with planar FET to prove that FINFET is much better.

Index Terms— Buried Oxide (BOX), Drain Induced Barrier Lowering (DIBL), MOSFET, Multiple Gates, Short Channel Effects, Silicon On Insulator (SOI), Threshold Voltage.

1 Introduction

Electronics is all about miniaturization. The invention of transistors revolutionized the electronic circuits. This revolution was further strengthened by invention of IC technology where many transistors were embedded on a single chip. Earlier BJTs were used in circuits but it was not feasible to embed many of them on a chip. This gave rise to the birth of FETs which had better performance parameters and comparatively smaller in size which enabled easy fabrication into a chip. Further developments in this regard lead to MOSFETs (Metal Oxide Semiconductor Field Effect Transistor). Scaling of planar MOSFETs over the past four decades has delivered ever-increasing transistor density and performance to integrated circuits (ICs). However, continuing this trend in the nanometer regime is very challenging due to the drastic increase in Short Channel Effects[1]. One of the biggest challenges for the VLSI circuits with higher technology nodes is to overcome the issue of catastrophic increases in power consumption due to short-channel effects caused from MOSFETs. Scaling of transistors to unimaginable level paved the way for the three dimensional FINFETs, promising potential to overcome many performance issues and limitation caused by planar MOSFETs.

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- *Author wish to thank Dr. K C NARASIMHAMURTHY Ph.D. (IITG) Professor & Head of Telecommunication engineering Department, Siddaganga Institute of Technology, Tumakuru-572103, for his support and courage given to formulate this Paper.*

2 Drawbacks of Mosfet

A channel is said to be long if its length is very much greater when compared with the depletion regions of source and drain. In this scenario the edge effect or the secondary effects are not taken into consideration. A channel is termed short whenever channel length is not larger than the sum of depletion width of source and drain. As channel length is reduced, departures from long channel behavior may occur. These departures, which are called Short Channel Effects, arise as results of a two-dimensional potential distribution and high electric fields in the channel region. For a given channel doping concentration, as the channel length is reduced, the depletion layer widths of source and drain junctions become comparable to channel length. The potential distribution in the channel now depends on both the transverse field E_x (controlled by the gate voltage and back-surface bias) and the longitudinal field E_y (controlled by the drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e. $E_x >> E_y$) is no longer valid. This two dimensional potential results in the degradation of the threshold behavior and introduces the Short Channel Effects which are listed below.

2.1 Channel Length Modulation

Channel length modulation in a MOSFET is caused by the increase of the depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length and an increased drain current. An example is shown in Figure-1. The channel length-modulation effect typically increases in small devices with low-doped substrates. An extreme case of channel length modulation is punch through effect where the charge carriers (either holes or electrons) start tunneling through from source to drain. As a result of tunneling effect sub-threshold leakage current (I_{OFF}) will increase which results loss of power when the transistor is in OFF state. During the

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ISSN 2229-5518

initial stage of channel length modulation output characteristics of MOSFET is as shown in Figure-2(a). At the worst case of channel length modulation sub-threshold slope increases, transistor drain current increases rapidly as shown in Figure-2(b).

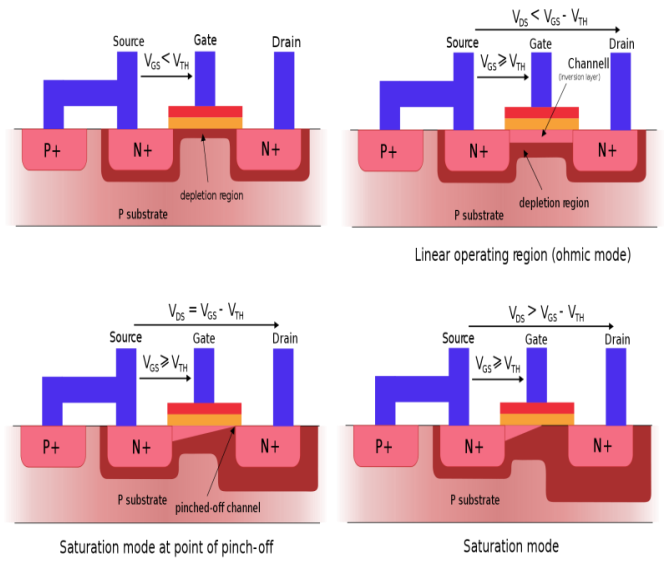

Fig. 1. Indicating shortening of channel length in Planar MOSFET.

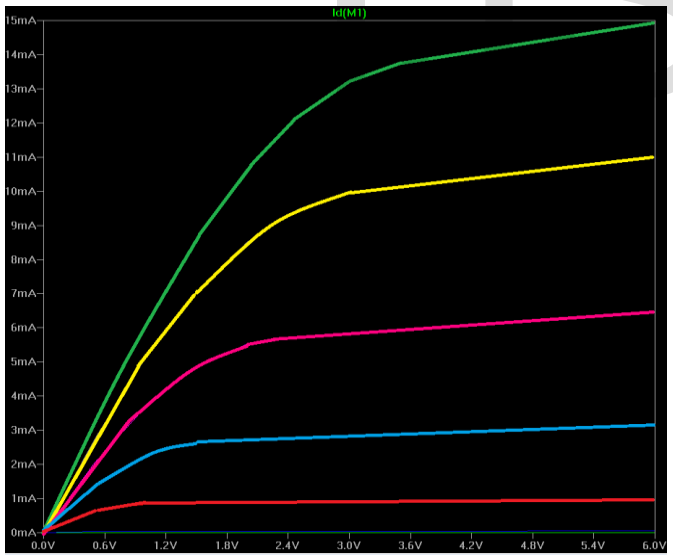

Fig. 2. Output characteristics of MOSFET simulated in LTspice software due to channel length modulation (a) During initial stage where there is small slope in the line of Output characteristics

As a result of channel length modulation transistor loses its linear property as shown in Figure-2. Hence a non-linear transistor will not have any application.

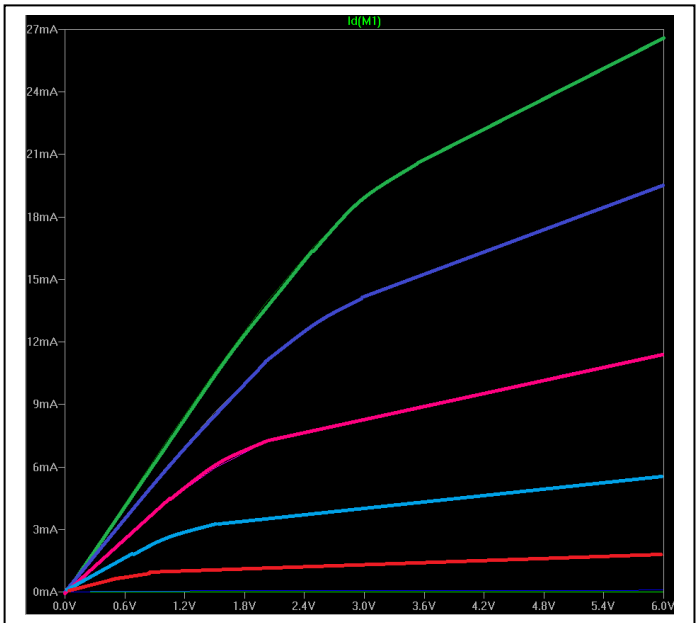

Fig. 2. Output characteristics of MOSFET simulated in LTspice software due to channel length modulation (b) At the extreme end stages where there is large slope in the curve of Output characteristics.

2.2 Threshold Voltage Variation with Channel Length Modulation

In case of long channel MOSFETs, gate has control over the channel and supports most of the charge. As we go to short channel lengths, the threshold voltage begins to decrease (as shown in Figure-3) as the charge in the depletion region is now supported by the drain and the source also. Thus the gate needs to support less charge in this region and as a result, Threshold voltage (V_{TH}) falls down. This phenomenon is known as charge sharing effect.

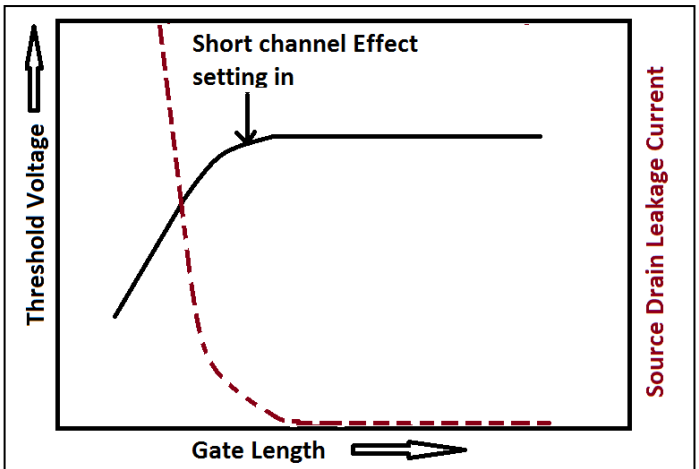

Fig. 3. Variation of Threshold voltage and source to drain leakage current with gate length

International Journal of Scientific & Engineering Research Volume 6, Issue 6, June 2015
ISSN 2229-5518

Now since I_{DS} is proportional to (V_{GS} - V_{Th}), therefore as V_{Th} begins to fall in case of short channels, I_{DS} starts increasing resulting in larger drain currents. When V_{GS} is zero and since V_{Th} is small, (V_{GS} - V_{Th}) will be a small negative value and will result in leakage current which further multiplied by the drain voltage will result in leakage current as shown in Figure-3. In case of long channel MOSFETs, V_{Th} is large enough and (V_{GS} - V_{Th}) is a comparatively larger negative value, in cut off mode leakage power is very small.

2.3 Drain Induced Barrier Lowering (DIBL)

DIBL is caused by the encroachment of the depletion region from the drain into the channel. The source and drain in effect take part of the channel charge, which would otherwise be controlled by the gate. At high drain bias, the depletion region strongly affects the channel potential so that it can actually interact with the source to channel junction and hence lowers the potential barrier. This problem is known as Drain Induced Barrier Lowering. When the source junction barrier is reduced, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current. As a result, the threshold condition can be reached at a lower gate voltage since the drain has already created a large portion of the depletion region. Strong DIBL is an indication of poor short channel behavior. However, since the transistor is not operated at a lower drain bias, DIBL itself is not a parameter that is directly related to circuit operation, but rather it is an indication of the degraded device characteristics.

3 FinFET Transistor

FinFETs have gained attention over the past decade because of the degrading short-channel behavior of planar MOSFETs. The heart of the FinFET is a thin (~10nm) Si fin. A heavily-doped poly-Si film wraps around the fin and makes electrical contact to the vertical faces of the fin. The poly-Si film greatly reduces the Source/Drain series resistance and provide a convenient means for local interconnect and making connections to the metal. The Wrap-around gate structure (shown in Figure-4) provides a better electrical control over the channel and thus helps in reducing the leakage current and overcoming other short-channel effects. A gap is etched through the poly-Si film to separate the source and drain. The conducting channel is wrapped around the surface of the fin. The Source/Drain and gate are much thicker (taller) than the fin, the device structure is not a planar structure but it's a 3D structure.

3.1 FinFET Fabrication

Sub-lithographic fins can be formed by using "spacers", formed along the sidewalls of a sacrificial patterned layer, as a hard mask (as shown in Figure-5). The width of the spacers is determined by the thickness of the deposited spacer layer, and can be very uniform across a wafer so that FinFET performance variability due to variations in fin width are minimized [2]. Another advantage of the spacer lithography process is that it provides for a doubling of fin density. After done with Fin formation further fabrication is same as MOSFET.

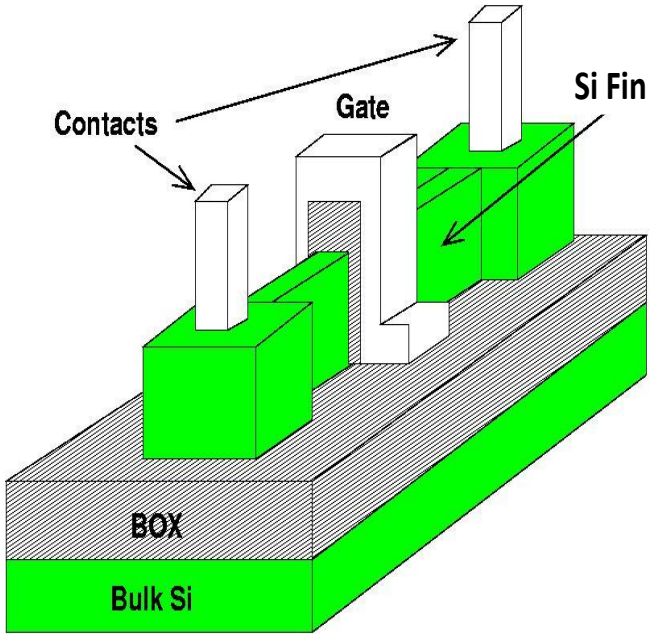

Fig. 4. Structure of FinFET, Showing Gate and Silicon Fin which acts as channel between two terminals of transistor. Metal contacts are given for two terminals.

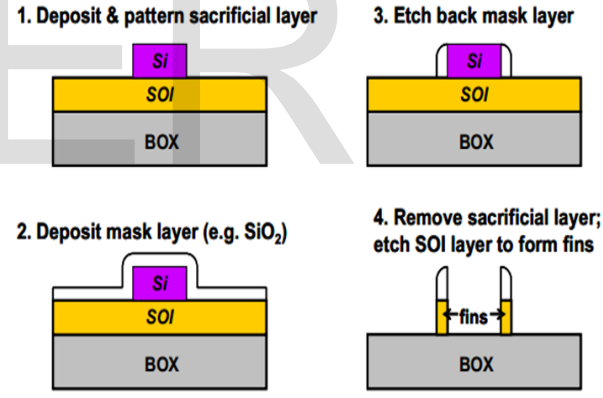

Fig. 5. Sequence of schematic cross-sections illustrating the process for forming fins with sub lithographic width using sidewall spacers.

Fin Design Considerations includes the distance of the fin (measured in the direction from source to drain) determines the effective channel length of the device. The channel width is basically twice the fin height (plus the fin width). FinFET channel (also known as the fin) is vertical. Hence, the height of the channel determines the width of the FinFET. This leads to a special property of FinFETs known as width quantization. This property says that the FinFET width must be a multiple of Fin Height, that is, widths can be increased by using multiple fins. Typically, fin height is determined by the process engineers and is kept below four times the fin thickness.

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ISSN 2229-5518

3.2 Advantages of FinFET Transistor

FinFET demonstrates the superior short-channel performance over planar MOSFETs with the same channel length. Since, the Fins are developed over either Buried Silicon Oxide (BOX) or over the substrate, Fin (act as a channel here) will not come into any disturbances caused by huge substrate. So, there are no issues like short channel effects [3] as we discussed in section II. Therefore, FinFET performances superior to MOSFET with respect to Drain Induced Barrier Lowering.

As we seen structure of FinFET in Figure-4, it can be observed that Fin is covered by three sides from gate, hence this is called Tri-Gate transistor. This construction helps the gate to have more and more control over the current flow along the Fin. Hence for lesser value of gate voltages we will get more amount of current as compared to MOSFET. Since in FinFETs there is no interaction between Fin and substrate it implies no channel length modulation. These superior output characteristic of FinFET over MOSFET is shown in Figure -6

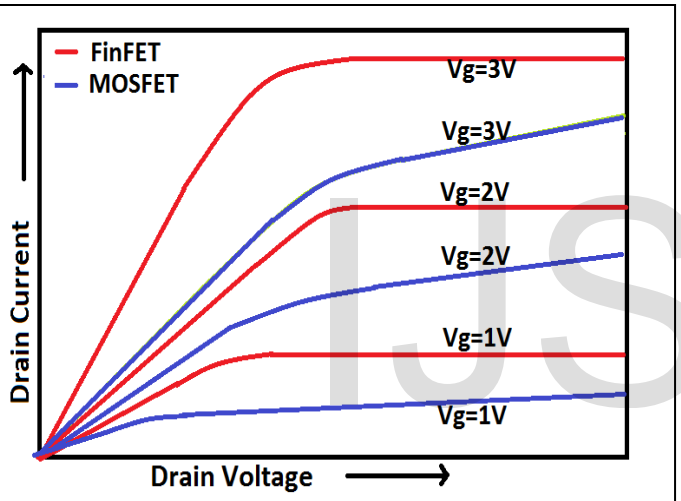

Fig. 6. Output Characteristics of FinFET and MOSFET for same amount of Gate voltages

Although FinFETs implemented on BOX, FinFETs implemented on conventional bulk wafers are more popular[4]. Figure-7 shows FinFETs implemented on bulk and BOX wafers. Some companies prefer the bulk technology because it is easier to migrate to bulk FinFETs from conventional bulk MOSFETs. However, FinFETs on both types of wafers are quite comparable in terms of cost, performance and it is premature to pick a winner.

4 Applications of FinFET Transistor

Intel, one of the leading companies in manufacturing processes for PCs and Laptops compared the performance of planar and 3D Tri-gate FinFET transistor. The structure of Planar and 3D transistor are as shown in Figure-8. Intel fabricated and simulated the results of 32nm planar, 22nm Planar and 22nm 3D transistors. Results show that 3D transistor performs better compared to planar transistors [5], which is as shown in Figure-9.

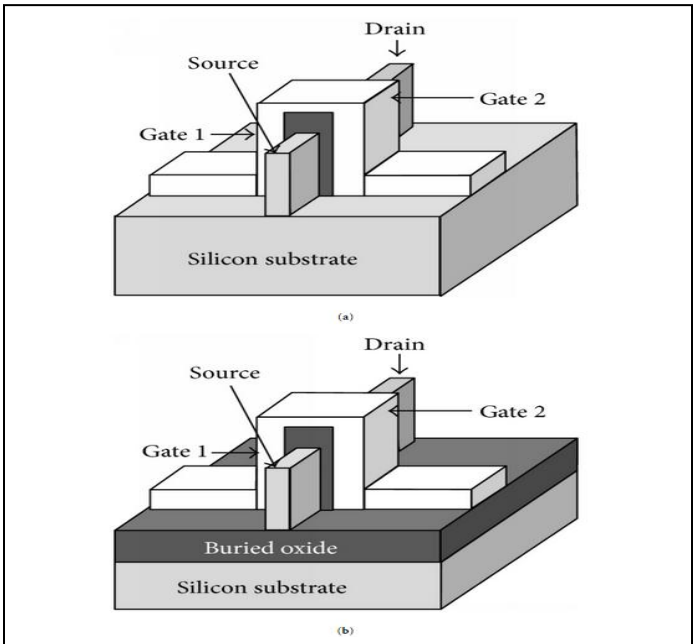

Fig. 7. Structural comparison between (a) bulk and (b) SOI FinFETs

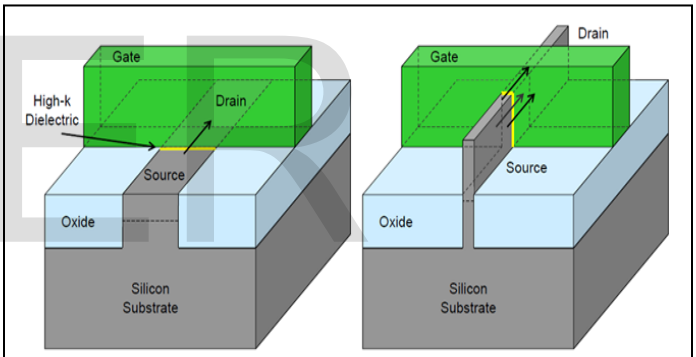

Fig. 8. Planar and Tri-Gate transistor

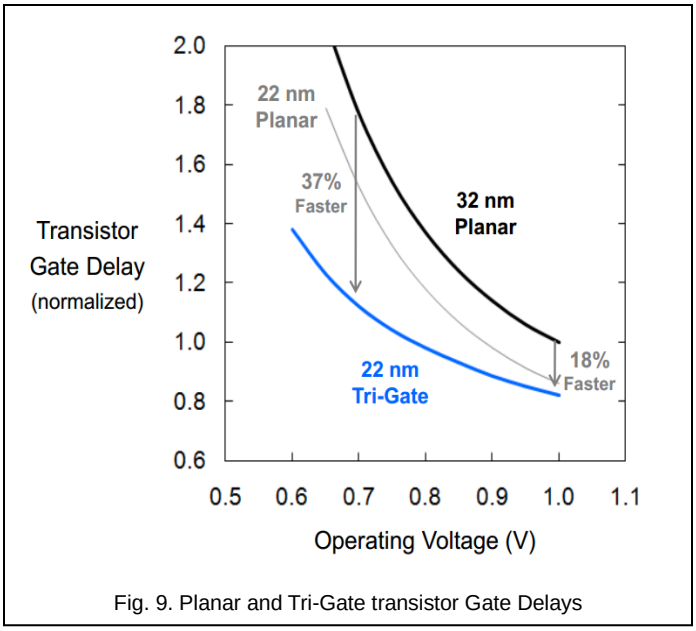

Fig. 9. Planar and Tri-Gate transistor Gate Delays

International Journal of Scientific & Engineering Research Volume 6, Issue 6, June 2015
ISSN 2229-5518

From the above result shown in Figure-9, Intel proved many advantages. They are; Dynamic performance of 22-nm Tri-Gate transistor is 37% faster than 32-nm Planar transistor at low voltage. Other than above results Intel also stated that more than 50% power reduction occurs at constant performance. Tri-Gate transistors Improves switching characteristics and also results higher drive current for a given gate voltage. Together with all above advantages, it is only 4% more costlier compared to planar transistor. Hence Intel is using only 3D FinFETs for processor development as sown in Table-I.

Generation	Processor Name	Release Date	Technology & Numbers	Speed (GHz)	Die Size (mm^2)
1	Nehalem	2008	42 nm HK-MG MOSFET 731 Million	1.8 - 2.6	684
2	Sandy Bridge	2011	32nm planar 1.27 Billion	2.4 - 3.6	270
3	Ivy Bridge	2012	22nm FinFET 1.86 Billion	3 - 4	256
4	Haswell	2013-14	22nm FinFET	3 - 4.6	177
5	Broadwell	Spring 2015	14nm FinFET		
6	Skylake	2H 2015	14nm FinFET		

Table-I: Intel's transistor technology for Processors to PCs and Laptops.

4 Conclusion

The new 3D Tri-gate FinFETs satisfy the requirements of mobile and high-performance computing applications, delivering a larger reduction in power consumption, higher switching performance and higher levels of integration than the previous generation planar transistor-based technologies. 3D Tri-gate FinFET devices will enable the continuation of CMOS scaling after conventional scaling has stalled and offers a tactical solution to the gate dielectric barrier and a strategic path for silicon scaling to the point where only atomic fluctuations halt further progress. Now, Intel is working on 3D Tri-gate FinFETs from last one decade and using the same for upcoming processors development in future (as depicted in Table-I) due to many advantages seen over planar MOSFET transistors. For both low-power and high-performance applications, 3D Tri-gate FinFET offers a most promising direction for continued progress in VLSI. Thus it can able to replace the existing planar FETs.

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